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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/903,208	TOPHAM, NIGEL PETER	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-15 and 30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-15 and 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4/8/02
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3, 5-15, and new claim 30 have been examined. Claims 16-29 have been withdrawn as per Applicant's request. Claims 2 and 4 have been cancelled as per Applicant's request. Claims 1, 3, 9, 10, 14, and 15 have been amended as per Applicant's request. New claim 30 has been added as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Amendment as received on 10 December 2004 and Request to Change Entity Status as received on 10 December 2004.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4 and 9-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Kissell, *MIPS16: High-Density MIPS for the Embedded Market.*

5. Regarding claims 1, 14 and 15, taking claim 1 as exemplary, Kissell has taught a processor adapted to receive instructions in one of:

a. First and second external instruction formats (see MIPS16 and MIPS, respectively, see p.4 lines 24-32), each instruction specifying one of a plurality of first operations executable by the processor or one of a plurality of second

operations executable by the processor, (see p.5 lines 10-13), the processor comprising:

i. At least one execution unit which receives instructions in an internal instruction format and executes the operations specified thereby (see p. 4 lines 29-35 and Fig. 3); and

ii. At least one instruction translation unit which translates each instruction received in at least one of said external formats into such an instruction in said internal format, the internal-format instruction specifying the same operation as the external-format instruction (see Fig.3 and p.4 lines 29-35). Here, the internal pipeline executes instructions in the standard MIPS architecture, with MIPS16 instructions being translated (decompressed) into MIPS instructions, and 32-bit MIPS instructions are translated using a "null translation" into MIPS instructions for execution in the pipeline.

b. Wherein each of said external format has one or more preselected opcode bits in which an opcode, specifying the same operation as the external-format instruction (see Fig.4, p.4 lines 30-32 and p.5 lines 10-13). Here, the definition of the opcode mapping between MIPS-I and MIPS16 instructions (as shown in Fig.4) is that a pre-selected portion of the opcodes in both instruction formats are defined to have identical bits (see the opcodes of Load Byte instruction in *Product Description: MIPS Application-Specific Extension*, p.26, cited as showing the definition of the opcodes and as authorized by the MPEP § 2131.01(II)).

c. At least one of said preselected opcode bit of said first external format is a common opcode bit which is also one of said preselected opcode bits of said second format (see Fig.4, p.4 lines 30-32 and p.5 lines 10-13);

d. Each of said first operation is specifiable in both said first and second external formats (see p.4 lines 30-32), and each of second operation is specifiable in said second external format (see Fig.4 and p.5 lines 10-13). Here, any MIPS16 operation is specifiable in both MIPS16 format and MIPS format. However, certain MIPS operations (i.e. those that use longer opcodes, a register that is un-specifiable in MIPS16 instruction format (due to one bit fewer in its source/target register fields), those that use longer immediate values, or those that require 64-bit data words) cannot be specified in the MIPS instruction format.

e. All of said first operations and all second operations have distinct opcodes in said second external format (see Fig.4 and p.5 lines 10-13). Here, because any MIPS16 operation can be specified in the MIPS instruction format, but not all MIPS operations can be specified in MIPS16, any first operation that is specifiable by MIPS16 and MIPS (and can be directly translated as in Fig.4) inherently has a different opcode than an instruction not specifiable in MIPS16, otherwise the two operations would be identical.

f. For every one of the first operations which the processor is capable of executing, the instruction specifying that operation in said first external format is identical, in each of said common opcode bit to the instruction specifying that operation in said second external format (see Fig.4, p.4 lines 30-32 and p.5 lines 10-13). Here,

the definition of the opcode mapping between MIPS-I and MIPS16 instructions (as shown in Fig.4) is that a pre-selected portion of the opcodes in both instruction formats are defined to have identical bits (see the opcodes of Load Byte instruction in *Product Description: MIPS Application-Specific Extension*, p.26, cited as showing the definition of the opcodes and as authorized by the MPEP § 2131.01(II)).

6. Claims 14, 15, and 30 are nearly identical to claim 1. Claim 14 differs in that it is comprised a machine-readable medium storing instructions to be executed, but its limitations encompass the same scope as claim 1. Claim 15 differs in that it is comprised as a method for encoding processor instructions, but its limitations also encompass the same scope as claim 1. Claim 30 differs in that it is comprised as a propagated signal embodying instructions executed by a processor, but its limitations also encompass the same scope as claim 1. Therefore, claims 14 and 15 are rejected for the same reasons as claim 1.

7. Regarding claim 3, Kissell has taught a processor as claimed in claim 1, also adapted to receive instructions in:

a. A third external instruction format (MIPS-III) (see p.4 lines 24-32 and p.5 lines 10-13),

b. Said third external format having one or more preselected opcode bits in which an opcode, specifying the operation to be executed, appears (see "major opcode" of MIPS-III instructions on p.5 lines 10-13), at least one of said preselected opcode bit of said third external format being a further common opcode bit which is also one of said preselected opcode bits of said second external format (see Fig.4, p.4

lines 30-32 and p.5 lines 10-13). Here, the definition of the opcode mapping between MIPS-I and MIPS16 instructions (as shown in Fig.4) is that a pre-selected portion of the opcodes in both instruction formats are defined to have identical bits (see the opcodes of Load Byte instruction in *Product Description: MIPS Application-Specific Extension*, p.26, cited as showing the definition of the opcodes and as authorized by the MPEP § 2131.01(II)). Because MIPS-III instructions are directly translatable and 100% fully compatible with MIPS-I instructions (see Col.4 lines 24-32 and Col.5 lines 10-13), the opcode bits that MIPS-I/II instructions have in common with MIPS-III instructions are inherently identical as well.

c. Wherein said execution unit receives instructions in at least one of first and second internal instruction formats and executes the operations specified thereby (see Fig.3 and p.4 lines 29-35). Here, the first internal format is considered to be what MIPS16 instructions are translated in, namely MIPS instructions using the MIPS16 Decompression Block (see Fig.3), and the second internal format is considered to be what MIPS-III instructions are translated into, also MIPS instructions, but using a "null translation".

d. Each of said second operations is specifiable in both said second and third external formats (see p.4 lines 24-32). Here, any MIPS16 operation is specifiable in MIPS16 instruction format, MIPS-I/II instruction format, and MIPS-III instruction format.

e. Said at least one instruction translation unit translates an instruction specifying said first operation in either said first or second external format into said first internal format, and translates instruction specifying said second operation in either said second or third external format into said second internal format (see Fig.3 and p.4 lines 29-35). Here, the first internal format is considered to be what MIPS16 instructions are translated in, namely MIPS instructions using the MIPS16 Decompression Block (see Fig.3), and the second internal format is considered to be what MIPS-III instructions are translated into, also MIPS instructions, but using a "null translation". Because a first operation (MIPS16) can be specified in MIPS16 or MIPS-I/II or MIPS-III formats, and a second operation (MIPS-I/II or MIPS-III) can be specified only in MIPS-I/II or MIPS-III formats, the first operation is translated into the format MIPS16 are translated into, and the second operation into the same format, although it is considered to be the format that MIPS-III instructions are translated into.

f. For every one of the second operations which the processors is capable of executing, the instruction specifying that operation in said second external format is identical, in each said further common opcode bit to the instruction specifying that operation in said third external formats (see Fig.4, p.4 lines 30-32 and p.5 lines 10-13). Here, the definition of the opcode mapping between MIPS-I and MIPS16 instructions (as shown in Fig.4) is that a pre-selected portion of the opcodes in both instruction formats are defined to have identical bits (see the opcodes of Load Byte instruction in *Product Description: MIPS Application-*

Specific Extension, p.26, cited as showing the definition of the opcodes and as authorized by the MPEP § 2131.01(II)). Because MIPS-III instructions are directly translatable and 100% fully compatible with MIPS-I instructions (see Col.4 lines 24-32 and Col.5 lines 10-13), the opcode bits that MIPS-I/II instructions have in common with MIPS-III instructions are inherently identical as well.

8. Regarding claim 9, Kissell has taught a processor as claimed in claim 1, wherein said first external format has an instruction width different from that of said second external format (see MIPS16 and MIPS, respectively, in Fig.4 and p.4 lines 24-29).

9. Regarding claim 10, Kissell has taught a processor as claimed in claim 1, wherein:

a. Said at least one translation unit (see MIPS16 Decompression Block in Fig.3) which performs a predetermined translation operation to translate each said external-format opcode into a corresponding internal-format opcode (see Fig.3 and p.4 lines 29-35). Here, the internal pipeline executes instructions in the standard MIPS architecture, with MIPS16 instructions being translated (decompressed) into MIPS instructions, and 32-bit MIPS instructions are translated using a "null translation" into MIPS instructions for execution in the pipeline.

10. Regarding claim 11, Kissell has taught a processor as claimed in claim 10, wherein said translation operation involves selecting and/or permuting bits amongst said preselected opcode bits in the external-format instruction (see Fig.4 and p.5 line 2 – p.6 line 2). Here, opcode bits of

the MIPS16 instructions are selected and mapped into the internal MIPS instruction format during translation.

11. Regarding claim 12, Kissell has taught a processor as claimed in claim 10, wherein the translation operation is independent of the external-format opcode (see Fig.4 and p.5 lines 10-13). Here, the translation is performed using a mapping, and thus is independent of the opcode value.

12. Regarding claim 13, Kissell has taught a processor as claimed in claim 12, wherein the translation unit identifies the internal format into which each external-format instruction is to be translated, and carries out said translation operation according to the identified internal format (see Figs.3-4, p.4 lines 30-33 and p.5 lines 10-13). Here, the MIPS16 Decompression Block identifies MIPS as the target internal format and translates MIPS16 instructions into MIPS instructions. Instructions that are already in uncompressed (MIPS) format can then be considered to use a "null translation" to be put into the internal format.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kissell, *MIPS16: High-Density MIPS for the Embedded Market,* as applied to claim 1 above, and further in view of Lin, U.S. Patent No. 6,633,969.

15. Regarding claim 5, Kissell has taught a processor as claimed in claim 1, but has not explicitly taught wherein the processor is a VLIW processor, wherein one external format is a scalar instruction format used for scalar instructions, and another external format is a VLIW instruction format used for VLIW instructions.

16. However, Lin has taught a VLIW processor with the ability to execute instructions in both long instruction word external formats (see Figs. 4B, 4D and Col.6 lines 12-48) and a scalar external formats (see Figs. 4A, 4C and Col.6 lines 12-48), allowing a 32-bit MIPS instruction to be produced every clock cycle so that processor throughput is increased (see Col.3 lines 1-16) while reducing the amount of storage space needed for the instructions (see Col.2 lines 1-39). One of ordinary skill in the art would have recognized that it is desirable to improve processor throughput, as well as to reduce instruction storage space required by a program. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Kissell to use VLIW instruction formats along with scalar instruction formats so that processor throughput can be increased and required storage space decreased.

17. Regarding claim 6, Kissell has taught a processor as claimed in claim 1, but has not explicitly taught wherein the processor is a VLIW processor, wherein the external formats are or comprise two different VLIW formats.

18. However, Lin has taught a VLIW processor with the ability to execute instructions in both long instruction word external formats (see Figs. 4B, 4D and Col.6 lines 12-48) and a scalar external formats (see Figs. 4A, 4C and Col.6 lines 12-48), allowing a 32-bit MIPS instruction to be produced every clock cycle so that processor throughput is increased (see Col.3 lines 1-16) while reducing the amount of storage space needed for the instructions (see Col.2 lines 1-39).

One of ordinary skill in the art would have recognized that it is desirable to improve processor throughput, as well as to reduce instruction storage space required by a program. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Kissell to use VLIW instruction formats along with scalar instruction formats so that processor throughput can be increased and required storage space decreased.

19. Regarding claim 7, Kissell in view of Lin has taught a processor as claimed in claim 6, wherein the two different VLIW formats are used in different respective instruction slots of a VLIW instruction parcel (see Fig. 4D). Here, the long instruction word parcel (instruction data block) contains both the 16-bit MIPS16 format (see Fig. 4B) as well as the 32-bit MIPS16 format (see Fig.4C) (see Col.6 lines 35-48)

20. Regarding claim 8, Kissell in view of Lin has taught a processor as claimed in claim 6, wherein at least one instruction slot of a VLIW instruction parcel uses the two different VLIW formats (see Fig. 4D). Here, the long instruction word parcel (instruction data block) contains both the 16-bit MIPS16 format (see Fig. 4B) as well as the 32-bit MIPS16 format (see Fig.4C) (see Col.6 lines 35-48).

Response to Arguments

21. Examiner withdraws objections to the specification in favor of the amended title and abstract.

22. Examiner withdraws the 35 U.S.C. 101 rejections in favor of the amended claims.

23. Examiner withdraws the 35 U.S.C. 112, first and second paragraph rejections in favor of the amended claims.

24. Applicant's arguments filed 10 December 2004 have been fully considered but they are not persuasive. Applicant argues in essence on pages 21-24

> However, the claims, as amended, now require that *for every one of the first operations (i.e. the operations which are specifiable in either external format) which the processor is capable of executing,* the instruction specifying that operation in the first external format is identical, in each of the common opcode bits, to the instruction specifying that operation in the second external format (page 22, paragraph 1).

25. This has not been found persuasive. The claim language, with claim 1 as exemplary, states "at least one of said preselected opcode bit of said first external format is a common opcode bit which is also one of said preselected opcode bits of said second external format". This means that the entire opcode does not need to be common, only one opcode bit needs to be in common for every one of the operations. In MIPS 16 and MIPS 32, at least one bit is in common. To follow the example given in the arguments on page 23, the SB MIPS16 instruction has an opcode of "110000" and the SB 32-bit MIPS instruction is "101000". The last three bits of the opcode are in common. All that is required by the claim language is that one bit is in common. Hence, the SB instruction meets the claim limitation. The claim language does not state that all of the opcode bits must be the same only that at least one bit must be the same. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., all opcode bits must match) are not recited in the rejected claim(s). Although the claims are interpreted in light of the

specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

26. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

27. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

29. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

30. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
18 February 2005

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SUPERVISORY PATENT EXAMINER
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